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Electrothermal effects in rf active devices
Measurement techniques and modeling

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Do not judge each day by the harvest you reap,
but by the seeds you plant.

Robert Louis Stevenson

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Chapter 1

Introduction

Today, very high operating frequencies and low power consumption are key features that drive the semiconductor market since the user demand has shifted toward wireless, compact and lightweight, broadband hand-held telecommunications equipment. These requirements can be only satisfied by steering away from the aged standard silicon process in favor of more suitable approaches.

One major drawback common to most modern rf technologies, though, lies in the devices being made of and surrounded by materials that exhibit low thermal conductivities, which drastically reduces the cooling efficiency of the active region. The trend toward progressively smaller geometries makes the situation even worse. Self-heating has therefore turned out to be a critical issue of foremost relevance affecting the design and operation of new devices and circuits.

Novel experimental techniques and simulation models are consequently devised as essential tools for investigating and predicting the dc/rf electrothermal behavior of high-frequency integrated transistors and evidencing a few peculiar effects due to

self-heating. The results attained prove definitely helpful to the researcher as well as to the designer.

With respect to on-chip circuits, besides the widespread and well-established digital technologies, integrated analog design is assuming fast-growing prominence in such fields as rf/microwave and optoelectronics as well as for magnetic storage applications. The latter represents the topic of an academic and industrial teamwork project, which resulted in the design of an innovative architecture for the analog front-end targeted to miniaturized (sized 1 inch or less) hard disk drives.

1.1 Modeling of electrothermal effects in rf bipolar transistors

The most recent active devices for radiofrequency and microwave, as well as power, applications suffer from rather evident self- and mutual heating effects, which can severely affect the ordinary operation. The main causes, to which the phenomenon can be traced back, can be identified as the continuous scaling down of the minimum feature size along with the high degree of electrical (and consequently thermal) isolation introduced, aimed at increasing frequency performance and reducing power consumption.

A detailed insight on thermal instability phenomena has led to the formulation of an analytical model capable of accurately predicting the critical points — and therefore the operating limits — in modern bipolar transistors (BJTs and HBTs). Such points are denoted as the voltage and current values on the device-under-test characteristics where either a

- *bifurcation* (multiple curve branching); or a

- *snap-back* (backward-bending curve, resulting in the presence of a negative resistance span); or even a

- *runaway* (presence of a vertical asymptote on the curve, in correspondence of which the control over current within the device is lost)

can be identified, once the dc biasing conditions are determined.

The study has highlighted the influence of the physical (self and mutual thermal resistances), geometrical and electrical (biasing scheme, choice of the asserted and driven quantities, possible presence of externally applied biasing resistors) parameters over the onset of electrothermal instabilities. On the overall, the analysis has therefore led to a better understanding of the mechanisms that regulate the phenomenon.

The results have been eventually generalized to multi-finger and multicellular devices made up of an arbitrary number of elementary units, where instabilities are determined by the complex pattern of interactions, both of electrical and thermal nature, between individual elements.

The formulation of the analytical model was supported by several FE (finite element) simulations and experimental measurements on devices fabricated on an insulating substrate (notably in silicon-on-glass technology). Moreover, a simulation core was implemented in a generic Spice environment by means of a modeling technique based upon behavioral blocks, known as ABM (analog behavioral modeling). A piece of software was also developed in Matlab environment, capable of solving the electrical and heat equations in totally coupled form for any driving case and bias level; the structure's thermal parameters are directly derived from the user input layout.

The development of the in-house produced software has required

overcoming several issues, partially raised by the intrinsic complexity of the strongly non-linear coupled equations and in some degree due to the presence of the critical points themselves, representing singular solutions to the equations, which the program is demanded to exactly identify. The simplified model adopted for the bipolar transistor's direct active region operation appears in the form of implicit equations that mutually relate the current gain (beta) and the collector current and link these quantities to junction absolute temperature as well. The model also accounts for high-injection regime effects, i.e., the decay of beta at the upper end of the current range, which is needed for an accurate representation of the re-stabilization region.

1.2 Experimental techniques for isothermal characterization of rf active devices

The above described simulation core and, more generally, commercial simulators require that the electrical parameters of the examined device are provided at a certain temperature, a procedure known as 'calibration'. Extracting the dc and small signal characteristics of an active device under isothermal conditions — whose equations temperature enters as a known constant parameter — is therefore a prerequisite demand.

From an experimental point of view, electrothermal measurement is the standard one since the dc-biased device under test are prone to heat up and exchange heat, especially when one deals with a multi-finger or multicellular transistor. Provided that the thermal feedback loop can not be broken up, then constant temper-

ature operation can be virtually attained only by short-pulse, long duty-cycle biasing, while externally forcing the temperature by means of a controlled heating/cooling element. Thus, it is apparent that a strict isothermal condition can not be assured — rather, this technique only yields an approximation: the shorter the pulses and the slower their repetition rate with respect to the thermal dynamics of the examined device, the better the isothermal condition is approached.

Therefore, this kind of measurement requires endowing the experimental setup with one or more power voltage pulse generators. Suitable commercial instruments are hardly available on sale and expensive: hence, considering the relative building simplicity of such pieces of equipment, the choice has naturally fallen onto designing and manufacturing two prototypes in house, tailored to the demand of the rf laboratory.

The whole development cycle has taken a few months of intense work. First, the programmable control logic was selected, based upon a microcontroller, rather than an FPGA, inasmuch as the former is inexpensive, rugged, widely available, reprogrammable at will with ease, endowed with a fast CPU and all the necessary peripherals internally. The logic was applied to a power section based on a low-resistance MOSFET supplied with its respective driver IC, and then completed with the proper support circuitry.

In the end, the overall measurement system was assembled by connecting several commercial discrete instruments together—a 67-GHz vector PNA (performance network analyzer), a probe station equipped with rf coplanar probes, a temperature-regulated chuck with a heating/cooling unit, a pulsed rf test set, a couple of pulsers and an oscilloscope for timing management and monitoring, two SMUs (source/measure units), a couple of pulsed-regime specific bias tees, a PC endowed with GPIB interface and laboratory

software—among which the in-house developed generators were placed, to form a unique high-performance experimental setup. The system was then tuned and tested by running a long batch of both dc and rf measurements.

1.3 Development of a low-power analog front-end for microdrive applications

A one-year teamwork with ST Microelectronics, although interrupted before completion, has resulted in the design of an SoC (system on chip) preamplifier for miniaturized hard disk drives.

The circuit has been developed upon very strict requirements for use in the ultra-portable device market. First, the electrical consumption is required to be very low in idle mode, only reaching the peak while writing data on disk. One more restriction is the limited space available. In order to meet the CompactFlash-II format geometrical specifications, the analog chip must be extremely small: on such reduced surface are to be placed the required support circuitry, a high-gain read LNA (low noise amplifier), the control logic with its serial interface channel, the write driver—the latter being deputed to supply the inductive write head with a current high enough to magnetize the target region on the memory medium.

One major concern is therefore obtaining a rather large current from a very low voltage, which can be solely attained by boosting the voltage to be applied to the head. Reaching the required data rate implies a special care to the switching edges handicapped by the flexible interconnect running between the preamplifier and the heads, which exhibits an uneven shape and is therefore characterized by a non-uniform impedance profile that introduces attenua-

tions and reflections in the current pulse.

Due to market requirements (compatibility with a wide range of heads and media), all the circuit parameters—voltages, currents, and durations—related to the magnetic and electric properties of the read/write subsystem have been designed to be thoroughly programmable. Moreover, the need of saving silicon usage has been accounted for: resorting to a very compact circuit layout and to a technology with an extremely tiny minimum feature size helped keeping silicon occupation, as well as power consumption, low.

Chapter 2

Modeling of electrothermal effects in rf bipolar devices

In this Chapter, thermal instability in multi-finger bipolar transistors is investigated in detail. Analytical models, electrothermal SPICE-based simulations and experimental measurements on silicon-on-glass transistors are used to study the mechanisms leading to current bifurcation in current-controlled devices. The analytical formulations include for the first time all the relevant parameters influencing the thermal instability onset such as series resistances, thermal coupling effects and current gain temperature dependence. Thus, a high accuracy degree is achieved with respect to previous simplified approaches. Besides, a novel SPICE electrothermal macromodel for bipolar transistors has been developed for dealing with the cases, when the simple analytical treatment is not adequate. SPICE simulations are used to substantiate the analytical models and to investigate complex device structures and unique phenomena occurring at high-current levels. The devel-

oped formulations are used to compare different technologies by varying the most significant parameters, thus demonstrating that silicon-germanium devices are more thermally stable than equivalent silicon ones and that thermally conducting substrates are needed to improve heat management.

2.1 Introduction

Self-heating effects may impose severe limitations on the electrical performance and reliability of bipolar transistors. When electrothermal feedback mechanisms are significant, different typologies of thermally-induced instability phenomena are observed, such as thermal runaway [1] and collapse of current gain [2], depending on the device nature (homojunction or heterojunction) and biasing conditions (voltage or current control).

The electrothermal behavior is noticeably complex in multi-finger structures, where the temperature profile and the current distribution are influenced by the thermal coupling between elementary transistors and by structural asymmetries. Nevertheless, thermal instability is detected even in two-finger devices controlled by base or emitter current, where in principle the geometrical symmetry should guarantee a uniform current distribution. Indeed, experience shows that, at certain critical biasing conditions, a current bifurcation is triggered: one of the fingers starts sinking the whole current, whereas the other tends to run dry. A measurement example is provided in Figure 2.1, where the schematic of a two-finger device driven by a base current I_{Btot} and a collector-emitter voltage V_{CE} is shown, along with a graph illustrating the typical behavior of the individual currents I_{C1} and I_{C2} as the total collector current increases.

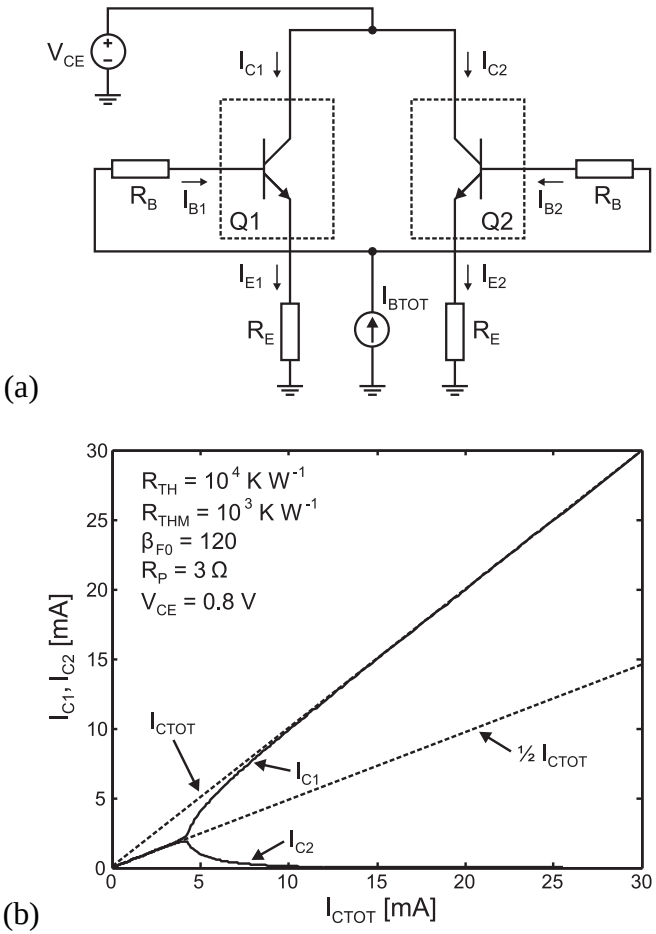


Figure 2.1 (a) Two-finger bipolar transistor driven by a total base current I_{Btot} and collector-emitter voltage V_{CE}. (b) Collector currents of individual fingers versus the total collector current for a typical two-finger silicon-on-glass NPN BJT.

Some attempts to analytically predict the uneven current distribution onset in two-finger transistors are reported in literature. A formula was early proposed by Winkler [3] and extended in more recent times to account for thermal coupling effects [4]. However, such expressions are derived from a first-order transistor model, which solely accounts for the influence of heating on collector current. A more accurate approach is presented in [5], where the electrothermal feedback is described by means of distinct effects on the base current and current gain. Yet, this analysis neglects thermal coupling, which is significant in practical multifinger structures.

In this Chapter, a novel and complete analysis of the electrothermal behavior of multifinger bipolar transistors is presented. Section 2.2 details the derivation of an analytical model to predict the biasing conditions leading to thermally-induced current bifurcation in ideally identical fingers (limit approach). As a starting point, the basic case of a two-finger device is investigated; the analysis is subsequently extended to multifinger transistors. Afterwards, the formulation developed for the two-finger structure is generalized to account for a small difference between chosen physical parameters of the transistor (perturbation model). For the first time, thermal coupling effects and current gain temperature dependence are simultaneously implemented. Such procedures are demonstrated to provide quite accurate results when predicting the onset of the unstable region. However, they are not suitable to account for more complex phenomena affecting the electrothermal behavior of multi-finger devices in a wide range of currents and temperatures.

A complete investigation of silicon BJTs is made possible through the introduction of a novel SPICE macromodel based on the ABM (analog behavioral modeling) approach, as detailed in

Section 2.3. The subcircuit representing an individual finger is derived from a model, which, despite its simplicity, thoroughly describes the relevant effects influencing the electrothermal behavior of bipolar transistors in forward active mode operation.

In Section 2.4, the analytical formulations are used to investigate the variation of the instability onset point following to changes in the physical device parameters, and also the electrothermal sensitivity of various device categories: both silicon and SiGe devices are characterized and a comparison is made between bulk silicon, silicon on insulator, silicon on glass [6]–[9], and silicon-on-copper [10] technologies. Several SPICE simulations are performed to validate the results. Excellent agreement with experimental data is achieved, even when describing high-current device operation.

All the experimental results presented are obtained from measurements performed on test structures made in back-wafer contacted silicon-on-glass NPN bipolar process [8]. Such structures are composed of a pair of identical NPN transistors with an individual emitter area $A_E = 20 \times 1\ \mu m^2$. The active regions are located in silicon mesas with a thickness equal to 0.74 μm, a width of 10 μm and a length varying from 50 to 100 μm, as schematically represented in Figure 2.2.

During silicon-on-glass processing, the bulk-silicon substrate is replaced by a glass wafer. The excellent electrical isolation of glass results in elimination of substrate losses, which, together with the low-ohmic front and back-wafer contacting, allows minimization of parasitics in active devices and enhanced integration with high-quality passives. However, the electrical advantages are counterbalanced by a severe drawback: the thermal resistance of transistors on glass is much higher than that of the corresponding bulk-silicon devices, due to the very low thermal conductivity of glass itself and the other materials surrounding the active

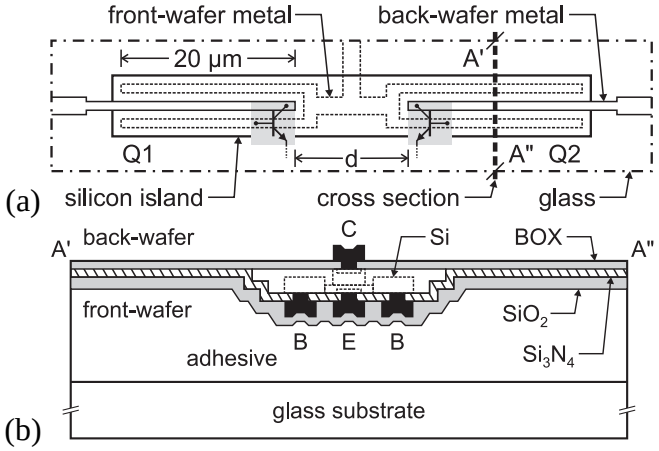


Figure 2.2 Schematic of the test structure fabricated in silicon-on-glass bipolar technology. (a) Top view. (b) Device section.

area. Self-heating and mutual thermal coupling resistances of the test structures are extracted using the lock-in measurement technique proposed in [11]. The values, given in Table 2.1, have been also verified by 3D numerical simulations performed through the commercial Femlab code [12]. Further details on silicon-on-glass process and devices are provided in [8].

Table 2.1 Experimental values for the self-heating and mutual thermal coupling resistances of the investigated test structures

Silicon island area [µm^2]	Silicon island thickness [µm]	R_{TH11} [K/W]	R_{TH12} [K/W]
50×10	0.74	15×10^3	9×10^3
80×10	0.74	13×10^3	2.5×10^3
100×10	0.74	10×10^3	1×10^3

All the measurements were performed on a Cascade probe station equipped with a temperature-controlled chuck and an HP4156B parameter analyzer.

2.2 Analytical formulations of thermal instability

Let us first refer to a single-finger device. A simple model that plainly describes the base current dependence on the "internal" base-emitter voltage and junction temperature in bipolar transistors operated in forward active mode is

$$I_B = I_{B0} \exp\left(\frac{V_{\mathrm{BE}int} + \varphi \Delta T}{\eta V_{T0}}\right) \tag{2.1}$$

where I_{B0} is a temperature-independent pre-exponential factor, $V_{\mathrm{BE}int}$ the voltage drop across the base-emitter junction, $\Delta T = T - T_0$ the temperature increase above ambient, $V_{T0} = kT_0/q$ the thermal voltage at room temperature, η the ideality factor, and

$$\varphi = -\left.\frac{\partial V_{\mathrm{BE}int}}{\partial T}\right|_{I_B}$$

the sign-changed temperature coefficient of the "internal" base-emitter voltage at a fixed base current. Note that the coefficient φ is positive, that is, the $V_{\mathrm{BE}int}$ needed to generate a certain I_B decreases with temperature. Such dependence can be easily explained at carrier level and is due to an increase of the intrinsic carrier concentration in the emitter with temperature. The term φ is commonly known as the thermo-electrical feedback coefficient, and is considered to be the most important factor influencing the electrothermal behavior of bipolar transistors [2], [13].

The "internal" base-emitter voltage $V_{\mathrm{BE}int}$ can be expressed as a function of the applied "external" V_{BE} as follows:

$$V_{\mathrm{BE}int} = V_{\mathrm{BE}} - R_B I_B - R_E(I_B + I_C) \tag{2.2}$$

where R_B and R_E are the base and emitter parasitic series resistances, respectively.

Substituting (2.2) into (2.1) yields

$$I_B = I_{B0} \exp\left(\frac{V_{\mathrm{BE}} + \varphi\Delta T - R_B I_B - R_E(I_B + I_C)}{\eta V_{T0}}\right) \tag{2.3}$$

which relates base and collector currents. Therefore, the introduction of the current gain β_F becomes somewhat compulsory. In general, β_F is dependent on temperature regardless of the bipolar transistor category. In silicon BJTs the gain increases with increasing temperature due to the band-gap narrowing in highly doped emitters, as described in early works [14], [15]. On the other hand, the gain in most HBTs exhibits a negative temperature coefficient due to the difference in the band-gaps between neighboring materials in the heterojunction, as investigated in GaInP/GaAs, AlGaAs/GaAs [16] and SiGe [17], [18] transistors.

Typically, the gain dependence on temperature can be accurately described through exponential relationships. However, accounting for another nonlinear law in addition to (2.3) would make the mathematical analysis troublesome and eventually unviable. Instead, one can resort to a linearized expression that well approximates the real gain behavior in a wide temperature range:

$$\beta_F(T) = \beta_F(T_0) + K_\beta(T - T_0) = \beta_{F0} + K_\beta\Delta T \tag{2.4}$$

as already proposed in [5] for AlGaAs/GaAs HBTs. Thus, the relationship between collector and base current becomes

$$I_C = (\beta_{F0} + K_\beta\Delta T)I_B \tag{2.5}$$

Let us now analyze devices composed of two "ideally identical" fingers. As schematically represented in Figure 2.3a, the temperature increase in the finger i is given by

$$\Delta T_i = P_{Di}R_{\mathrm{TH}} + P_{Dj}R_{\mathrm{THM}} \approx V_{\mathrm{CE}}I_{Ci}R_{\mathrm{TH}} + V_{\mathrm{CE}}I_{Cj}R_{\mathrm{THM}} \qquad (2.6)$$

where $i, j = 1 \ldots 2$ $(i \neq j)$, V_{CE} is the collector-emitter voltage, and R_{TH} and R_{THM} the self-heating and mutual thermal coupling resistances between fingers, respectively. Hence, the current gain can be expressed as

$$\beta_{Fi}(T) = \beta_{F0} + K_\beta V_{\mathrm{CE}}(I_{Ci}R_{\mathrm{TH}} + I_{Cj}R_{\mathrm{THM}}) \qquad (2.7)$$

which, after substituting I_{Ci} and I_{Cj} with the corresponding right-hand side of (2.5), becomes

$$\beta_{Fi}(T) = \beta_{F0} + K_\beta V_{\mathrm{CE}}[I_{Bi}\beta_{Fi}(T)R_{\mathrm{TH}} + I_{Bj}\beta_{Fj}(T)R_{\mathrm{THM}}] \qquad (2.8)$$

The solution of the system composed by (2.8) and the analogous equation for the finger j is given by

$$\beta_{Fi}(T) = \frac{\beta_{F0}[1 - K_\beta V_{\mathrm{CE}}I_{Bj}(R_{\mathrm{TH}} - R_{\mathrm{THM}})]}{S} \qquad (2.9)$$

being $S = 1 - K_\beta V_{\mathrm{CE}}(I_{Bi} + I_{Bj})R_{\mathrm{TH}} + K_\beta^2 V_{\mathrm{CE}}^2 I_{Bi}I_{Bj}(R_{\mathrm{TH}}^2 - R_{\mathrm{THM}}^2)$.

Equation (2.3) can be rearranged so that for the finger i it becomes equal to

$$\eta V_{T0} \ln\left(\frac{I_{Bi}}{I_{B0}}\right) = V_{\mathrm{BE}} + \varphi\Delta T_i - R_B I_{Bi} - R_E[I_{Bi} + \beta_{Fi}(T)I_{Bi}] \quad (2.10)$$

By combining (2.10) with (2.6) and (2.9), after some algebra, we

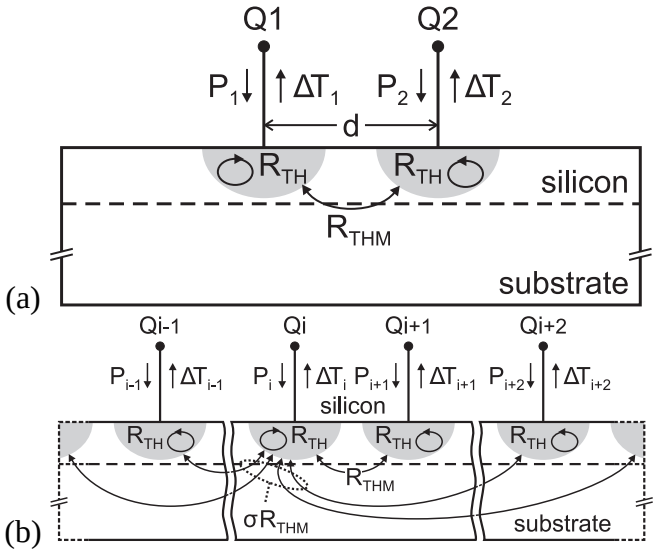


Figure 2.3 Scheme of the thermal coupling between (a) two elementary devices; (b) N elementary devices.

obtain

$$\eta V_{T0} \ln\left(\frac{I_{Bi}}{I_{B0}}\right) = V_{\mathrm{BE}} + \\ + I_{Bi} \frac{\beta_{F0}[1 - K_\beta V_{\mathrm{CE}} I_{Bj}(R_{\mathrm{TH}} - R_{\mathrm{THM}})]}{S} (\varphi V_{\mathrm{CE}} R_{\mathrm{TH}} - R_P) + \\ + I_{Bj} \frac{\beta_{F0}[1 - K_\beta V_{\mathrm{CE}} I_{Bi}(R_{\mathrm{TH}} - R_{\mathrm{THM}})]}{S} \varphi V_{\mathrm{CE}} R_{\mathrm{THM}} \tag{2.11}$$

with

$$R_P \approx R_E + \frac{R_B}{\beta_{F0} + 1}$$

Subtracting from (2.11) the analogous expression written for the

finger j yields

$$\ln\left(\frac{I_{Bi}}{I_{Bj}}\right) = (I_{Bi} - I_{Bj})\frac{\beta_{F0}}{\eta V_{T0} S}[\varphi V_{\mathrm{CE}}(R_{\mathrm{TH}} - R_{\mathrm{THM}}) - R_P] \qquad (2.12)$$

This expression relates the base currents of the fingers i and j, and holds both for the situation in which the two base currents are identical and for the situation in which they are different.

2.2.1 The limit approach

To find the boundary between symmetry and asymmetry in the base current distribution, we first assume that the currents are unequal, and then let them tend to each other, i.e. $I_{Bi} \rightarrow I_{Bj}$. Equation (2.12) is rearranged in the following way:

$$I_{Bj} = \frac{\ln\left(\frac{I_{Bi}}{I_{Bj}}\right)}{-\left(1 - \frac{I_{Bi}}{I_{Bj}}\right)\frac{\beta_{F0}}{\eta V_{T0} S}[\varphi V_{\mathrm{CE}}(R_{\mathrm{TH}} - R_{\mathrm{THM}}) - R_P]} \qquad (2.13)$$

and L'Hôpital's rule is applied to find the limit for $I_{Bi}/I_{Bj} \rightarrow 1$. This procedure leads to an expression for the critical base current at the bifurcation point:

$$I_{Bcrit} = \frac{\eta V_{T0} S'}{\beta_{F0}[\varphi V_{\mathrm{CE}}(R_{\mathrm{TH}} - R_{\mathrm{THM}}) - R_P]} \qquad (2.14)$$

where $S' = 1 - I_{Bcrit}(2K_\beta V_{\mathrm{CE}} R_{\mathrm{TH}}) + I_{Bcrit}^2[K_\beta^2 V_{\mathrm{CE}}^2(R_{\mathrm{TH}}^2 - R_{\mathrm{THM}}^2)]$.

For $\varphi V_{\mathrm{CE}}(R_{\mathrm{TH}} - R_{\mathrm{THM}}) - R_P \neq 0$, (2.14) yields

$$A_0 I_{Bcrit}^2 + B_0 I_{Bcrit} + C_0 = 0 \qquad (2.15)$$

where

$$A_0 = K_\beta^2 V_{\mathrm{CE}}^2 (R_{\mathrm{TH}} - R_{\mathrm{THM}})(R_{\mathrm{TH}} + R_{\mathrm{THM}})$$
$$B_0 = -2K_\beta V_{\mathrm{CE}} R_{\mathrm{TH}} - \frac{\beta_{F0}}{\eta V_{T0}} [\varphi V_{\mathrm{CE}} (R_{\mathrm{TH}} - R_{\mathrm{THM}}) - R_P]$$
$$C_0 = 1$$

The solution of the square equation defined by (2.15) is the base current of an individual finger at the bifurcation point. The critical collector current I_{Ccrit} can be evaluated through (2.9). The total base/collector current leading to current bifurcation is calculated by multiplying individual currents by two.

By assuming a temperature-insensitive current gain (i.e., $K_\beta = 0$), one obtains

$$\frac{\beta_{F0} I_{Bcrit}}{\eta V_{T0}} [\varphi V_{\mathrm{CE}} (R_{\mathrm{TH}} - R_{\mathrm{THM}}) - R_P] = 1 \tag{2.16}$$

and therefore

$$I_{Ccrit} = \frac{\eta V_{T0}}{\varphi V_{\mathrm{CE}} (R_{\mathrm{TH}} - R_{\mathrm{THM}}) - R_P} \tag{2.17}$$

The further hypothesis of a negligible thermal coupling between fingers leads to

$$I_{Ccrit} = \frac{\eta V_{T0}}{\varphi V_{\mathrm{CE}} R_{\mathrm{TH}} - R_P} \tag{2.18}$$

The limit approach can be generalized for multi-finger transistors under some assumptions through the following straightforward procedure. Let us consider an N-finger device, with fingers $1, 2, \ldots, i-1, i, i+1, \ldots, N-1, N$ as in Figure 2.3b, and assume that the electrothermal behavior of the i-th finger is significantly affected only by the two adjacent (left and right) fingers, which happens in most practical situations. Under this assumption, (2.6) can

be rewritten for the couple composed of the i-th and the $(i + 1)$-th finger as

$$\Delta T_i = V_{\mathrm{CE}} I_{Ci} R_{\mathrm{TH}} + V_{\mathrm{CE}} I_{C(i-1)} R_{\mathrm{THM}} + V_{\mathrm{CE}} I_{C(i+1)} R_{\mathrm{THM}} \tag{2.19}$$

$$\Delta T_{i+1} = V_{\mathrm{CE}} I_{Ci} R_{\mathrm{THM}} + V_{\mathrm{CE}} I_{C(i+1)} R_{\mathrm{TH}} + V_{\mathrm{CE}} I_{C(i+2)} R_{\mathrm{THM}} \tag{2.20}$$

being R_{TH} and R_{THM} the self-heating thermal resistance of an individual finger and the mutual thermal coupling resistance between neighboring fingers, respectively.

Let us assume that the instability onset starts in the i-th finger, while all other fingers carry the same current, say $I_{C(i+1)}$. Equations (2.19) and (2.20) then become

$$\Delta T_i = V_{\mathrm{CE}} I_{Ci} R_{\mathrm{TH}} + 2 V_{\mathrm{CE}} I_{C(i+1)} R_{\mathrm{THM}} \tag{2.21}$$

$$\Delta T_{i+1} = V_{\mathrm{CE}} I_{Ci} R_{\mathrm{THM}} + V_{\mathrm{CE}} I_{C(i+1)} (R_{\mathrm{TH}} + R_{\mathrm{THM}}) \tag{2.22}$$

Applying algebraic manipulations as before, it is demonstrated that the base current of individual fingers at the current bifurcation point in multifinger transistors can be calculated through the following square equation

$$A_1 I_{Bcrit}^2 + B_1 I_{Bcrit} + C_1 = 0 \tag{2.23}$$

where

$$A_1 = K_\beta^2 V_{\mathrm{CE}}^2 (R_{\mathrm{TH}} - R_{\mathrm{THM}})(R_{\mathrm{TH}} + 2R_{THM})$$

$$B_1 = -K_\beta V_{\mathrm{CE}} (2R_{\mathrm{TH}} + R_{\mathrm{THM}}) - \frac{\beta_{F0}}{\eta V_{T0}} [\varphi V_{\mathrm{CE}} (R_{\mathrm{TH}} - R_{\mathrm{THM}}) - R_P]$$

$$C_1 = 1$$

It should be noted that (2.23) describes exactly the case of an infinite number of fingers, where every finger is ideally surrounded

by two fingers (one on the left and one on the right). In principle, (2.23) is inadequate when considering the case of a few fingers operated in parallel. Indeed, in this situation, the electrothermal behavior may be dominated by the outmost devices (which do not have fingers on one side) that start to conduct current lower than other transistors at I_B values well below the ones predicted by (2.23). On the other hand, the accuracy degree is acceptable for a large number of fingers.

Equation (2.23) is based on the assumptions of uniform thermal interaction (i.e., uniform spacing) between adjacent fingers and $R_{\mathrm{THM}ij} = 0$ when $|i - j| > 1$. In a more general situation, the thermal coupling degree between any finger of the couple i, $i + 1$ and all other fingers is described by σR_{THM}, being R_{THM} the mutual thermal resistance between i and $i+1$ (see Figure 2.3b). This leads to the following general relationships:

$$\Delta T_i = V_{\mathrm{CE}} I_{Ci} R_{\mathrm{TH}} + V_{\mathrm{CE}} I_{C(i+1)} (1 + \sigma) R_{\mathrm{THM}} \tag{2.24}$$

$$\Delta T_{i+1} = V_{\mathrm{CE}} I_{Ci} R_{\mathrm{THM}} + V_{\mathrm{CE}} I_{C(i+1)} (R_{\mathrm{TH}} + \sigma R_{\mathrm{THM}}) \tag{2.25}$$

yielding

$$A_\sigma I_{Bcrit}^2 + B_\sigma I_{Bcrit} + C_\sigma = 0 \tag{2.26}$$

where

$$A_\sigma = K_\beta^2 V_{\mathrm{CE}}^2 (R_{\mathrm{TH}} - R_{\mathrm{THM}})[R_{\mathrm{TH}} + (1 + \sigma) R_{\mathrm{THM}}]$$

$$B_\sigma = -K_\beta V_{\mathrm{CE}} [2R_{\mathrm{TH}} + \sigma R_{\mathrm{THM}}] - \frac{\beta_{F0}}{\eta V_{T0}} [\varphi V_{\mathrm{CE}} (R_{\mathrm{TH}} - R_{\mathrm{THM}}) - R_P]$$

$$C_\sigma = 1$$

The coefficient σ defines the weight of the thermal coupling between the fingers i, $i+1$ and the surrounding fingers. Depending on the value of σ, an arbitrary situation can be effectively described, in particular

- when the couple i, $i + 1$ is thermally isolated, that is, the fingers are coupled two by two in the multifinger device;

- when the weight of the thermal coupling degree between adjacent fingers is uniform and the thermal interaction between non-neighboring fingers is negligible.

2.2.2 The perturbation model

The I_{Bcrit} value given by (2.15) is evaluated under the assumption of identical fingers. However, this contrasts with the fact that thermal instability cannot arise in the ideal case, when the two fingers are identical. In order to achieve (2.15), a mathematical trick was adopted: first, it was assumed that in a certain region the base currents are different, and then the limit was evaluated, where they equalize. Actually, regardless of the way a two-finger transistor is designed in order to ensure perfect symmetry, there will be still some difference between the fingers (e.g., in doping, in layout, in contact resistance or in any other process parameter, or most likely in many of them at a time), which is—however small—enough to trigger the current bifurcation phenomenon.

Let us analyze the measured characteristics in Figure 2.4. As can be seen, the bifurcation does not occur abruptly. Rather, it exhibits a gradual behavior, depending on the magnitude of the difference between the fingers. Thus, a more general way of defining the thermal instability point is

$$\delta I_{Ci} = 0. \tag{2.27}$$

In order to study the actual bifurcation point behavior, a small discrepancy is assumed to exist between the fingers. In the present analysis, a perturbation in the series resistance is introduced: finger j exhibits a reduction in series resistance by an amount of ΔR_P,

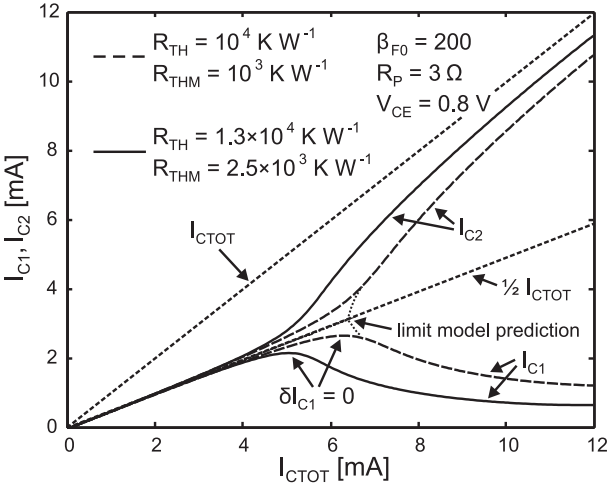


Figure 2.4 Measured (solid) current bifurcation mechanism in two-finger silicon-on-glass BJTs along with the curves (dotted) evaluated via (2.13).

with respect to finger *i*. [1] Hence, (2.11) can be rewritten for the case of finger *j* as follows:

$$\eta V_{T0} \ln\left(\frac{I_{Bj}}{I_{B0}}\right) = V_{\mathrm{BE}} + \\ + I_{Bj}\frac{\beta_{F0}[1 - K_\beta I_{Bi} V_{\mathrm{CE}}(R_{\mathrm{TH}} - R_{\mathrm{THM}})]}{S}[\varphi V_{\mathrm{CE}} R_{\mathrm{TH}} - (R_P - \Delta R_P)] + \\ + I_{Bi}\frac{\beta_{F0}[1 - K_\beta I_{Bj} V_{\mathrm{CE}}(R_{\mathrm{TH}} - R_{\mathrm{THM}})]}{S}\varphi V_{\mathrm{CE}} R_{\mathrm{THM}}. \tag{2.28}$$

Note that (2.11) still holds for finger *i*. Subtracting (2.28) from

[1] Noteworthy is, that similar approaches might be attempted, based on the perturbation of other physical parameters such as R_{TH}, K_β, β_{F0}, and so on.

(2.11) then yields

$$\ln\left(\frac{I_{Bi}}{I_{Bj}}\right) = (I_{Bi} - I_{Bj})\frac{\beta_{F0}}{\eta V_{T0} S}[\varphi V_{\mathrm{CE}}(R_{\mathrm{TH}} - R_{\mathrm{THM}}) - R_P] - \\ -\frac{\beta_{F0}\Delta R_P}{\eta V_{T0} S} I_{Bj}[1 - K_\beta V_{\mathrm{CE}} I_{Bi}(R_{\mathrm{TH}} - R_{\mathrm{THM}})]. \tag{2.29}$$

This equation relates the base currents and can be conveniently written in the following form:

$$\ln\left(\frac{I_{Bi}}{I_{Bj}}\right)[1 - (I_{Bi} + I_{Bj})D + I_{Bi} I_{Bj}(D^2 - E^2)] = \\ = (I_{Bi} - I_{Bj})F - I_{Bj}[1 - I_{Bi}(D - E)]G, \tag{2.30}$$

where

$$D = K_\beta V_{\mathrm{CE}} R_{\mathrm{TH}}, \qquad E = K_\beta V_{\mathrm{CE}} R_{\mathrm{THM}},$$
$$F = \frac{\beta_{F0}}{\eta V_{T0}}[\varphi V_{\mathrm{CE}}(R_{\mathrm{TH}} - R_{\mathrm{THM}}) - R_P], \qquad G = \frac{\beta_{F0}\Delta R_P}{\eta V_{T0}}.$$

Finally, differentiation of (2.30) and application of the instability onset criterion (2.27) lead to [2]

$$\frac{1}{I_{Bj}}[1 - D(I_{Bi} + I_{Bj}) + I_{Bi} I_{Bj}(D^2 - E^2)] + \\ + \ln\left(\frac{I_{Bi}}{I_{Bj}}\right)[D - I_{Bi}(D^2 - E^2)] = F + G - G(D - E) I_{Bi}. \tag{2.31}$$

Equations (2.30) and (2.31) represent a nonlinear system, whose solution in terms of $I_{Bi\,crit}$ and $I_{Bj\,crit}$ can be obtained in a numerical fashion.

[2] Device *j*, characterized by a smaller series resistance, tends to draw the whole current, whereas device *i* gradually turns off.

2.3 A SPICE-based macromodel for electrothermal simulation of Si BJTs

Both approaches proposed in Section 2.2 offer a convenient technique for evaluating the thermal instability point in current controlled multi-finger bipolar transistors. However, only circuit simulation programs based on accurate electrothermal and thermal models can provide an in-depth investigation of the electrothermal behavior of such devices in a wide range of operating conditions. Unfortunately, most commercial tools widely used in the IC CAD area, such as SPICE, are in principle unsuited to the purpose, since the temperature of the entire circuit is assigned prior to simulation and remains constant independently of the dissipated power. Thus, self-heating of individual devices and thermal coupling are not accounted for.

The method usually adopted to enable SPICE for electrothermal simulations is the structural macromodeling technique, which starts from the built-in device model as main element, and adds supplementary passive and active standard components in order to describe specific device phenomena. An effective alternative is the analog behavioral macromodeling, which makes use of a powerful facility introduced in latest SPICE versions: some of the laws governing the electrical and thermal device behavior can be easily modeled by means of voltage-controlled voltage (ABM) and current (ABM/I) sources that allow a straightforward "in line" implementation of a large variety of algebraic equations.

The effectiveness of this approach for the electrothermal simulation of power MOSFETs and BJTs has been demonstrated in literature [19], [20]: the developed macromodels prove flexible and accurate, and yet require analysis times in the same order of magnitude as when using standard SPICE elements. Lastly, it is well

worth noting that ABM-based electrothermal subcircuits are manageable in all the modern SPICE-like simulation codes supporting the ABM facilities.

In this Section, a novel ABM-based macromodel is proposed for the electrothermal analysis of multifinger silicon BJTs. The subcircuit representation for the elementary device is entirely derived from a simple, yet accurate model, which has been successfully applied to the simulation of power vertical transistors [21] and is based on the separate description of the base current and current gain.

2.3.1 The base current

In the analysis of Section 2.2, the temperature coefficient of the internal base-emitter voltage φ is assumed to be constant. Nevertheless, in general this parameter is a function of base current and a weak function of temperature [21]. This can be accurately described by means of the logarithmic law

$$\varphi(I_B) = \varphi_0 - \varphi_1 \ln\left(\frac{I_B}{I_{B0}}\right), \tag{2.32}$$

where the fitting parameters φ_0 and φ_1 are easily extracted from the measured $V_{\mathrm{BE}int}$ versus junction temperature characteristics for several I_B values.

Substituting (2.32) into (2.1) yields

$$I_B = I_{B0} \exp\left(\frac{V_{\mathrm{BE}int} + \varphi_0 \Delta T}{\eta V_{T0} + \varphi_1 \Delta T}\right), \tag{2.33}$$

which guarantees a higher accuracy compared to the formulation expressed by the sole (2.1).

2.3.2 The current gain

As will be shown in the next Section, the assumption of a linearized gain dependence of temperature is accurate enough when detecting the bifurcation onset. However, in order to analyze of the electrothermal behavior in a wide range of temperatures and currents, the temperature dependence should be more adequately modeled through an exponential relationship, and the gain collapse due to high-injection effects is to be taken into account.

The following half-heuristic expression is adopted for beta:

$$\beta_F(I_C,T)=\beta_{F0}\frac{\exp\left[-\dfrac{\Delta E_G(N_E)}{k}\left(\dfrac{1}{T}-\dfrac{1}{T_0}\right)\right]}{1+\left(\dfrac{I_C}{I_H}\right)^{n_H}}, \tag{2.34}$$

where $\Delta E_G(N_E)$ is the doping-dependent band-gap narrowing in the emitter, and I_H, n_H are model parameters to describe the beta lowering at high current regimes. [3]

2.3.3 The SPICE macromodel

The electrothermal SPICE macromodel based on (2.33) and (2.34) is displayed in Figure 2.5 for a BJT laid out in common-emitter configuration. The subcircuit representing the single-finger transistor is evidenced (dashed line). As can be seen, besides the standard input/output quantities, an additional input ΔT (the temperature increase above ambient, treated as a voltage) and a supple-

[3] Noticeably, in silicon BJTs the gain fall-off is more pronounced than in HBT counterparts. Indeed, in the latter only the Kirk effect ordinarily occurs, whereas the Webster effect (high injection levels in the base) is uncommon because of the high base doping concentration.

mentary output P_D (the dissipated power, computed as a current) are considered. The diode is used to describe the internal base-emitter junction behavior. Since this intrinsic SPICE device is characterized by a constant temperature during the whole simulation run, it draws a temperature-independent current given by

$$I_{Bdiode} = I_B(V_{\mathrm{BE}int}, T_0) = I_{B0} \exp\left(\frac{V_{\mathrm{BE}int}}{\eta V_{T0}}\right). \tag{2.35}$$

In order to obtain a temperature-dependent base current in accordance with (2.33), the ABM/2I block *A* is adopted, which evaluates and forces a *correction current*

$$\begin{aligned} &I_{Bcorr}(V_{\mathrm{BE}int}, \Delta T) = \\ &= I_{B0}\left[\exp\left(\frac{V_{\mathrm{BE}int} + \varphi_0 \Delta T}{\eta V_{T0} + \varphi_1 \Delta T}\right) - \exp\left(\frac{V_{\mathrm{BE}int}}{\eta V_{T0}}\right)\right] \end{aligned} \tag{2.36}$$

that is then added to the diode current (2.35).

The ABM/2 block *B* generates a voltage corresponding to the gain β_F, which is computed from I_C and ΔT according to (2.34). The collector current I_C is, in turn, calculated through the ABM/2I block *C* by simply multiplying the base current $I_B = I_{Bdiode} + I_{Bcorr}$ by the gain.

It should be noted that the proposed macromodel allows accounting for the effect of external resistors, denoted by the *ext* subscript. When considering the common-emitter configuration, the dissipated power P_D is evaluated within the subcircuit by the ABM/2 block *G* as

$$P_D = V_{\mathrm{BE}dev} I_B + V_{\mathrm{CE}dev} I_C, \tag{2.37}$$

being

$$\begin{aligned} V_{\mathrm{BE}dev} &= V_{\mathrm{BE}int} + R_{Eint} I_E + R_{Bint} I_B, \\ V_{\mathrm{CE}dev} &= V_{\mathrm{CE}ext} - R_{Cext} I_C - R_{Eext} I_E. \end{aligned}$$

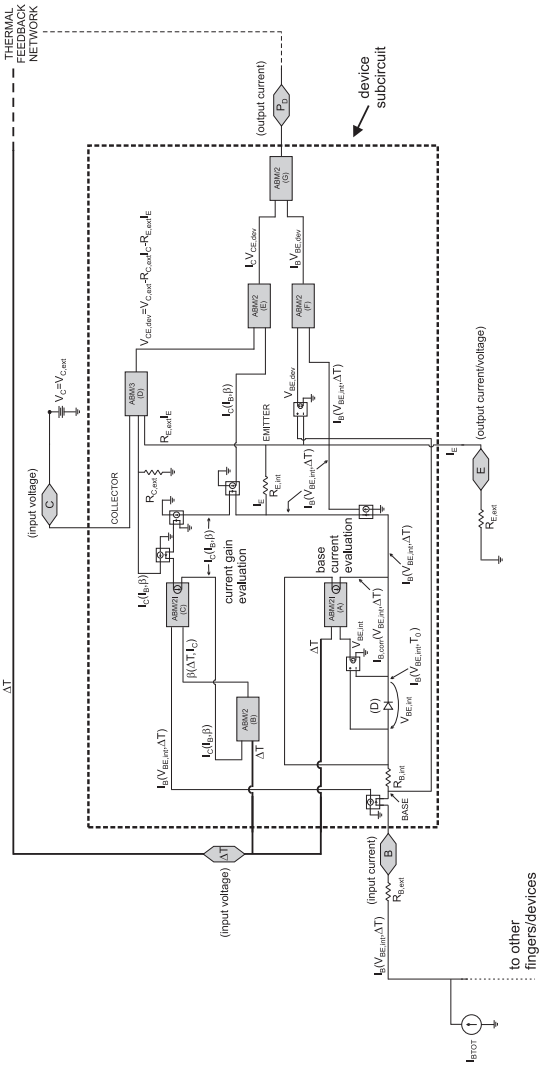


Figure 2.5 Detailed diagram of the ABM-based SPICE macromodel for BJTs. The subcircuit corresponding to a single transistor is also evidenced (dashed).

Power P_D is an input variable entering the thermal feedback network, represented by an equivalent electrical network. In the case of an N-finger device, the temperature increase above ambient corresponding to the i-th transistor is given by:

$$\Delta T_i = \sum_{j=1}^{N} R_{\mathrm{TH}ij} P_{Dj}, \tag{2.38}$$

where thermal resistances are treated as electrical.

2.4 Results and discussion

In this Section, the parameters of the analytical models are varied and their influence on the bifurcation point is studied. In addition, the accuracy of the proposed formulations is evaluated through comparisons with SPICE simulations and electrical measurements.

As a first step, the perturbation model is used in order to examine the effect of a non negligible difference ΔR_P between the series resistances on the biasing and temperature conditions that trigger the instability. It is clear that, when ΔR_P is set to zero, the values calculated by the perturbation model are the same as those drawn from the limit model. In this investigation, ΔR_P is varied from 0 to 0.5 Ω. In Figure 2.6, the total collector current at the onset of thermal instability is plotted for three collector-emitter voltages along with the corresponding temperature difference between the fingers. It is apparent that the total current does not change significantly, whereas the difference in temperature—and consequently in collector currents—between the fingers increases with larger ΔR_P. Therefore, the perturbation model should clearly supersede the simplified limit approach when a detailed analysis of the individual fingers at the critical point is required.

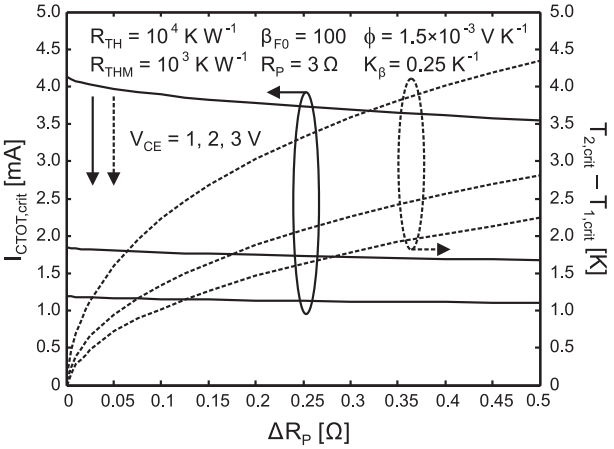


Figure 2.6 Critical collector current and temperature difference between individual fingers versus ΔR_P for three collector-emitter voltage values (perturbation model).

Figure 2.7a shows the SPICE characteristics I_{C1}, I_{C2} as functions of I_{Ctot} for three ΔR_P values, along with the individual currents evaluated at the instability point through the perturbation model. As can be seen, a good agreement is obtained, despite the intrinsic higher accuracy of the SPICE macromodel. In a similar fashion, Figures 2.7b and 2.7c demonstrate that the perturbation model is suited to correctly predicting the SPICE calculated thermal instability occurrence for various values of K_β and R_{TH}, respectively.

The limit model is used for evaluating the bifurcation onset in two-finger devices as a function of R_P, R_{TH}, R_{THM} and K_β. The influence of varying internal series resistance on the thermal instability point is shown in Figure 2.8. It is well known [3], [22] that the critical current increases as the series resistance grows higher. If no parasitic or external series resistance lowers the base-emitter

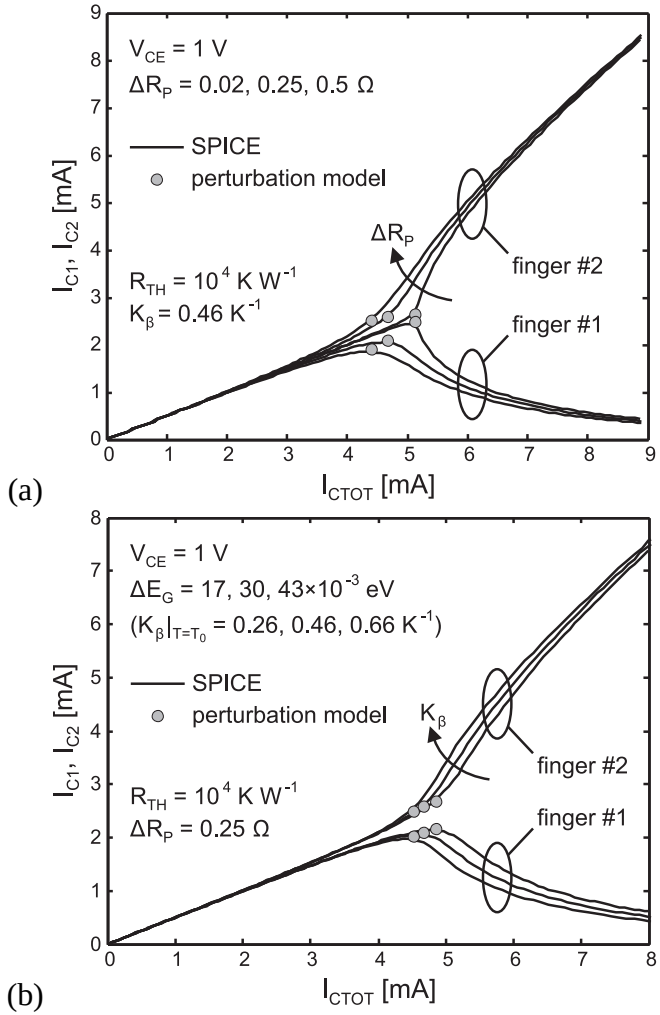
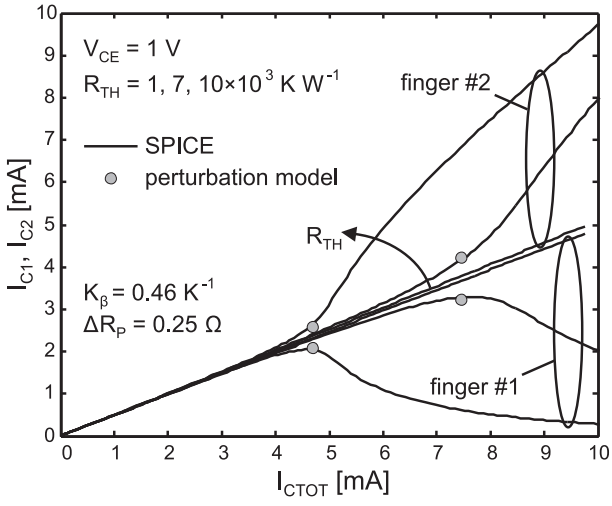


Figure 2.7 Comparison between SPICE simulation (solid) and perturbation model (symbols). Effect of varying (a) ΔR_P and (b) K_β.



(c)

Figure 2.7 (continued) Comparison between SPICE simulation (solid) and perturbation model (symbols). Effect of varying (c) R_{TH}.

junction voltage, the temperature increase at thermal instability is roughly bias-independent. This behavior is similar to that observed for single-emitter devices at the onset of thermal runaway [9]. Differently from the data presented in Figure 2.6, the temperature increase above ambient shown in Figure 2.8 is the same for both fingers, since the simplified limit model was applied. Noticeably, although an increase of the series resistance improves the electrothermal stability of a bipolar transistor, such an approach is not attractive for rf designers since it degrades the high-frequency performance. Therefore, other ways for optimizing the electrothermal behavior of a rf device are to be sought, such as introduction of on-wafer heat spreaders [8], silicon substrate thinning [23], [24], different packagings and substrate transfer [7].

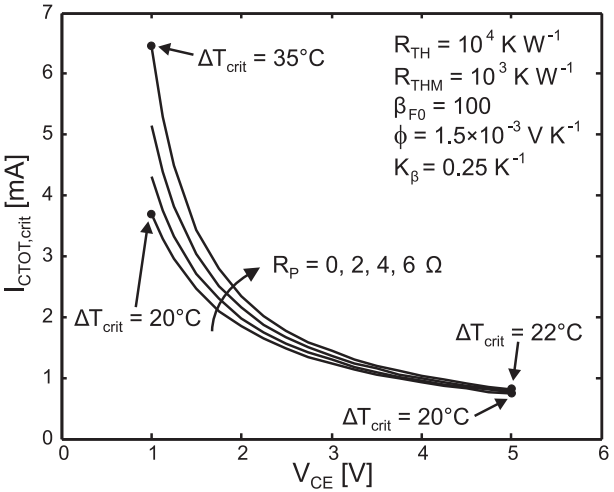


Figure 2.8 Critical collector current and corresponding temperature increase calculated through the limit model as functions of the collector-emitter voltage for various series resistance values.

The influence of the temperature dependence of current gain on thermal instability is investigated by varying the coefficient K_β from -1 to 1 K^{-1}. The chosen range exactly covers the typical values for silicon-germanium ($-1 \leqslant K_\beta < 0$ K^{-1}) and silicon ($0 < K_\beta \leqslant 1$ K^{-1}) transistors with current gains around 100. For this analysis, the self-heating and mutual thermal coupling resistances are numerically calculated using Femlab and silicon-on-glass, silicon-on-insulator, bulk-silicon and silicon-on-copper technologies are compared. The simulated devices are characterized by an emitter area of $2 \times (20 \times 1)$ μm^2.

With reference to Figure 2.2, distance d is set to 10 μm while the top-silicon thickness is taken equal to 1 μm. The 300-μm substrate is modeled in turn as

1. a thermally insulating glass substrate,

2. a poorly thermally conducting silicon-on-insulator substrate with buried oxide thickness $t_{BOX} = 0.4$ μm,

3. a thermally conducting silicon substrate, and

4. a highly thermally conducting copper substrate.

The calculated self-heating and mutual thermal coupling resistances are given in Figure 2.9, where both the critical collector current and the corresponding temperature increase at the onset of thermal instability (calculated by the limit model) are shown for each of the four technologies. Figure 2.10 illustrates the influence of the mutual thermal coupling resistance (i.e. the finger pitch d) on the critical values of collector current and temperature. The results clearly demonstrate that taking into account both the temperature dependence of current gain and mutual thermal coupling resistance between fingers is essential. The devices with a current-gain negative temperature coefficient like SiGe and AlGaAs/GaAs HBTs are by far more thermally stable than silicon BJT counterparts—that is, their dissipated power at the point of instability onset is greater. One can conclude that, from the point of view of thermal behavior, negative K_β technologies on thermally conducting substrates (e.g., silicon-on-copper [10]) represent a better choice.

Yet, it has been observed that even silicon bipolar transistors may exhibit a negative temperature coefficient (NTC) behavior in the current gain, when they are operated at high collector currents. Indeed, isothermal measurements performed on silicon-on-glass devices have shown that, at high current regimes, the positive temperature coefficient (PTC) behavior induced by the band-gap

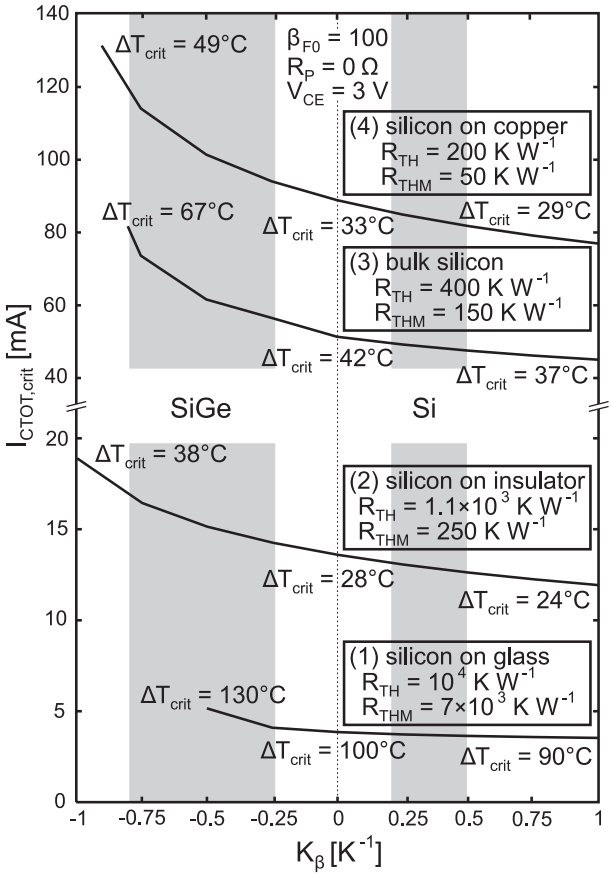


Figure 2.9 Thermal instability in $2 \times (20 \times 1)$ µm^2 NPN bipolar transistors with 10-µm finger pitch in different technologies (limit model).

narrowing phenomenon turns into an NTC as illustrated in Figure 2.11a, where experimental data are compared to (2.34) after proper parameter calibration. This is due to the temperature de-

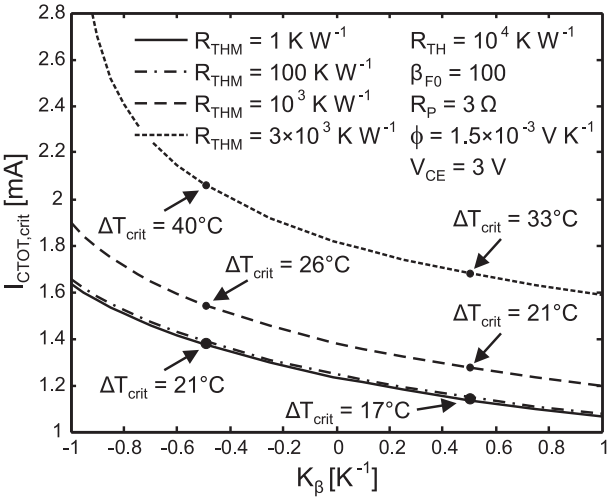


Figure 2.10 Critical collector current and corresponding temperature increase calculated through the limit model versus the current gain temperature coefficient for various mutual thermal resistance values.

pendence of the current levels leading to high-injection effects. It is apparent that such mechanism plays a key role in the electrothermal behavior of multifinger silicon transistors working under high-current conditions. Note that an accurate description of the PTC to NTC transition through the zero temperature coefficient (ZTC) region can be obtained by simply considering linear temperature dependence laws for I_H and n_H. An enhanced version of the SPICE macromodel that takes into account this effect is therefore straightforwardly available.

As an application, the electrothermal behavior of the test structure depicted in Figure 2.2 is investigated in a wide range of current values for various distances d between the fingers. The mea-

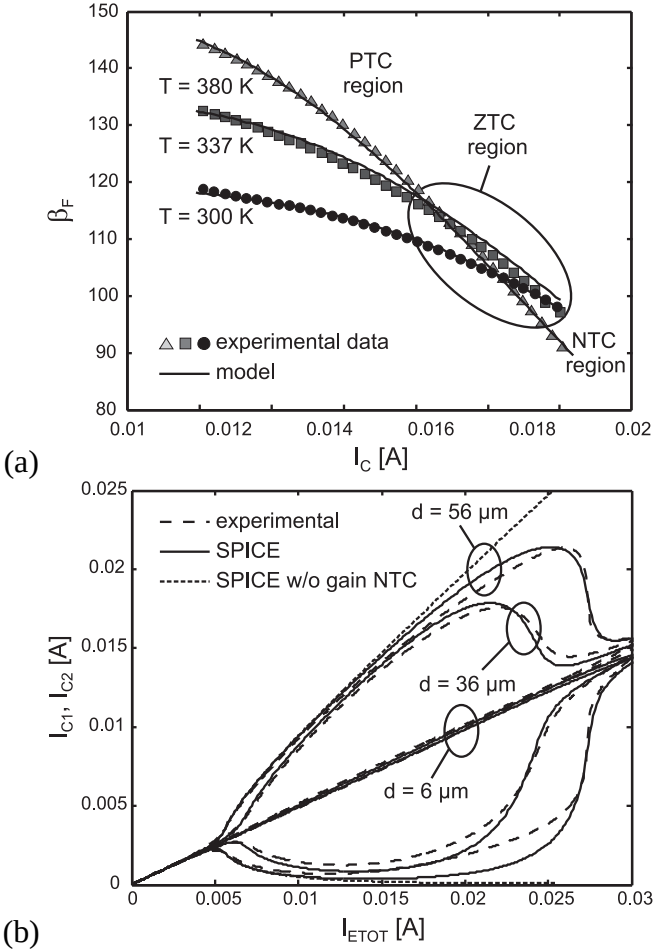


Figure 2.11 (a) Current gain as a function of collector current at various substrate temperatures for a typical silicon-on-glass BJT: comparison between measurements (symbols) and calibrated model (2.34) (solid). (b) Electrothermal behavior of two-finger devices characterized by different distances between individual fingers: comparison between measurements (dashed) and SPICE simulations (solid and dotted).

surements are performed by increasing the total emitter current I_{Etot} in dc (non-isothermal) mode at $V_{CB} = 0$ V. The experimental data are shown in Figure 2.11b. As can be seen, the more the devices are 'thermally uncoupled', that is, the larger the distance between the fingers is, the more easily the current bifurcation takes place. However, an unexpected, yet desirable stabilizing effect is observed at large emitter currents, where the collector currents tend to become equal again.

SPICE simulations have been performed using the above described approach. The values adopted for self-heating and mutual thermal coupling resistances are shown in Table 2.1. Both the asymmetry onset and the stabilizing mechanism are correctly described for each value of d. The instability is induced by introducing a small difference between the transistors connected in parallel. For the sake of completeness, an illustrative SPICE simulation is performed without accounting for the temperature dependence of the parameters I_H and n_H: as depicted in the same figure, the hotter finger suddenly carries the whole current and the stabilizing mechanism does not arise. A comprehensive and accurate SPICE-enabled diagnostics of the overall behavior is therefore possible with short simulation times and no convergence issues.

The presented SPICE approach is easily extendable to an arbitrary multi-finger transistor. As an example, the case of a three-finger BJT, whose top view is shown in Figure 2.12, has been investigated. The spacing between the fingers is assumed uniform. The chosen values for self-heating and mutual thermal coupling resistances are typical of silicon-on-glass devices:

$$R_{TH11}, R_{TH22}, R_{TH33} = R_{TH} = 10.5 \times 10^3 \text{ K/W},$$
$$R_{TH12}, R_{TH21}, R_{TH23}, R_{TH32} = R_{THM1} = 5 \times 10^3 \text{ K/W},$$
$$R_{TH13}, R_{TH31} = R_{THM2} = 2 \times 10^3 \text{ K/W}.$$

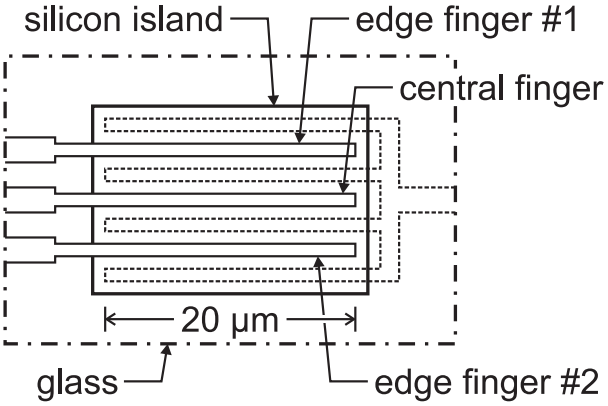


Figure 2.12 Top view of the simulated three-finger device.

The total emitter current has been increased, while keeping a fixed collector-base voltage $V_{\mathrm{CB}} = 0.75$ V. The collector currents versus I_{Etot} are shown in Figure 2.13. Continuous lines refer to the case of identical fingers, that is, under perfectly balanced conditions. As apparent from the graph, a thermally-induced unevenness in the current distribution arises at low/medium I_{Etot} levels: the innermost finger starts conducting more and more current owing to the strong thermal coupling with both neighboring devices, which handle the same amount of current because of the ideally perfect system symmetry. Nevertheless, at high current levels, the system approaches a stable situation, since the central finger eventually enters the NTC region of current gain. A more complex behavior is detected when introducing a slight discrepancy in the internal emitter resistances ($\Delta R_{Eint} = 0.1\ \Omega$) between the outmost fingers. As can be seen, when $I_{Etot} = 15 \times 10^{-3}$ A, the applied unbalancing condition gives rise to a current bifurcation between these fingers as well. Owing to its higher collector current positive tempera-

ture coefficient, edge finger #1 sucks down some current from the central finger. Then, for current values larger than 27×10^{-3} A, the effect of the introduced ΔR_{Eint} somewhat fades away, due to the stabilizing concurrence of the gain negative temperature coefficient in both the central and the hotter side finger.

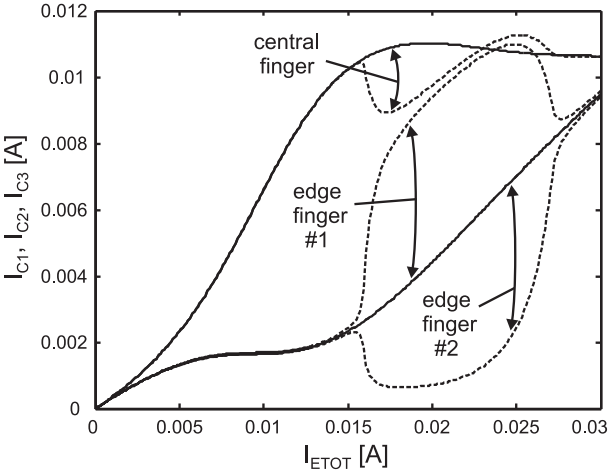


Figure 2.13 SPICE simulated electrothermal behavior of a three-finger device. The case of ideally identical fingers (solid) is compared to the more realistic unbalanced side fingers case (dashed).

2.5 Conclusions

The electrothermal behavior of multifinger bipolar transistors has been thoroughly studied in this Chapter. Based on a simple bipolar transistor model, an analytical formulation of the critical current leading to thermal instability has been derived as a function of

device parameters for two ideally identical fingers and generalized to the case of multi-finger transistors. The two-finger analysis is subsequently extended to account for a slight difference between fingers. For the first time, thermal coupling and beta temperature dependence have been taken into account at the same time.

For a complete prediction of the electrothermal behavior of devices with an arbitrary number of fingers, a novel ABM-based SPICE macromodel has been presented. The analytical formulations have been used for studying the thermal stability of bipolar transistors that exhibit opposite temperature dependence of the current gain. Moreover, the effect of different substrate materials has been analyzed. It has been demonstrated that silicon-germanium technology on highly thermally conducting substrates results in superior electrothermal performance. The analytical prediction of the thermal instability occurrence has been substantiated by electrical measurements on silicon-on-glass bipolar transistors and electrothermal SPICE simulations in a wide range of physical parameter values.

Chapter 3

The dc/rf pulsed measurement system

Chapter 4

Design of a low-power analog front-end for microdrives

This Chapter proposes the design of an enhanced driver for magnetic storage write heads to be employed in mini- and microdrive applications. It is intended for running from a reduced-voltage supply (as commonly found in portable devices) with low power consumption, yet retaining an excellent write speed performance, and is thoroughly programmable. Although originally developed in BiCMOS technology, the design is compatible with a full CMOS process. The original schedule planned the whole front-end to be engineered: the project was stopped before completion, though, reaching the stage where the sole write driver was fully designed.

4.1 Introduction

A challenging request from the mobile equipment market is an ever larger storage capability on phones, music players and hand-

held PCs with more and more reduced weight, size, power consumption and cost. In order to face this growing demand, new technologies have to be adopted in magnetic storage along with a deeper integration of the electronic subsystems.

In Figure 4.1, the internals of a 1-inch CompactFlash-II format microdrive are detailedly illustrated, while the read/write subsystem schematic layout is represented in Figure 4.2. It is clearly visible that the heads are connected to the preamplifier chip via a transmission line, namely a flexible (or suspension) interconnect, which is responsible for a number of inconveniences encountered in engineering the chip. Being made up of heterogeneous segments with bends and corners, in fact, the flex — as it is commonly termed — exhibits an irregular shape and consequently an impedance profile that cannot be even nearly taken as uniform or easily matched.

Figure 4.3 displays the inner structure of the preamplifier chip, whose specifications are listed as follows.

- Dual-channel SoC (system on chip) manufactured in CMOS065 technology (80 nm minimum feature size);

- power supply: +3 V/ – 2 V dual (read channel), 3 V single ended (write channel plus control logic);

- operation guaranteed down to +2.4 V/ – 1.7 V (20% off the nominal values);

- 250 Mbit/s data rate;

- head compatibility: GMR/TMR (read), thin-film inductive (write);

Figure 4.1 Exploded drawing detailing the internals of a CF-II size miniaturized hard disk drive. The artwork is reproduced by courtesy of Griff Wason. Copyright ©2003 Griff Wason.

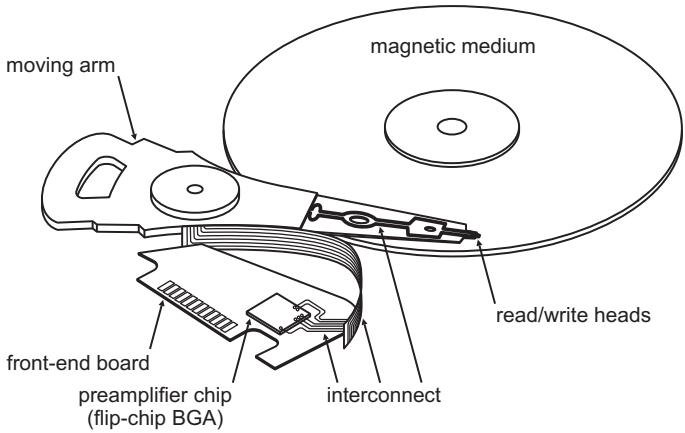


Figure 4.2 Components of the read/write subsystem in a miniaturized hard disk drive.

- compliance with a wide range of heads and media: all parameters (currents, durations, gains, impedances, LFCs, waveforms) are thoroughly programmable;
- featuring a 50 Mbit/s syncronous serial control interface;
- ultra low-power design: reduced supply voltage, low average consumption, SLEEP/READ/WRITE workstates;
- suitability for perpendicular recording drives.

One of the most troublesome issues to cope with in miniaturized hard disk drives is the availability of only a low-voltage single-ended power supply (typically, a battery), which urges for new circuit solutions to be sought after, especially in those sections where relatively high currents are required. This applies therefore to the write driver, as being the front-end directly deputed to drive large

currents into the inductive head in order to generate the adequate magnetic excitation.

In order to overcome the magnetic inertia of the head-airgap-substrate system and be able to swiftly invert its magnetic induction, a high current peak is initially required (overshoot). Current can then be reduced for the subsequent bits to be written (minimum coercitive magnetic field) until next inversion occurs, as qualitatively displayed in Figure 4.4.

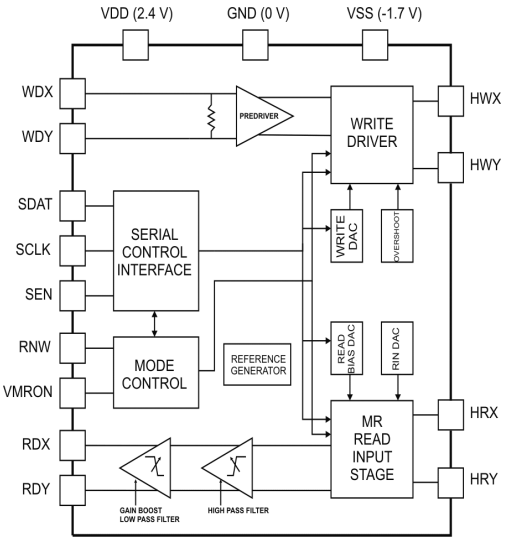


Figure 4.3 Block diagram of the complete preamplifier chip.

Several preamplifier designs were lately proposed [25]–[27], along with the earlier [28], [29], all of which realized either in bipolar or BiCMOS technology, working at 5 V or higher and devised for the best speed performance at the expense of power consumption. A first approach to a full CMOS write driver was undertaken in [30]; again, power saving is less than a priority issue. In

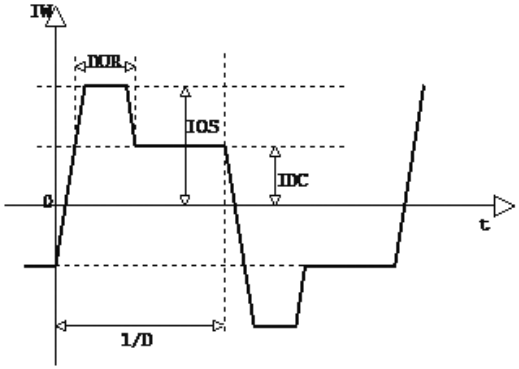


Figure 4.4 Qualitative current waveform in the write head.

less recent times, a low-power preamplifier in bipolar technology [31] was demonstrated for a 3.3-V minimum supply, but the specifications are by far outdated in view of modern designs. Only the latest [32] explicitly addresses the low-voltage low-power case.

The inductive-head driver design presented here is specifically targeted to mini- and micro-drives and supersedes former circuits under several aspects. Based on ST Microelectronics patents [33], [34], with a bunch of core improvements aimed to make it suitable for mobile appliances, it runs from as low as a 3-V single-ended supply with reduced power consumption. The write speed can be raised up to a maximum of 500 Mbit/s, which is well beyond the requirements of the ultra-portable range.

The driver is fully programmable as to both the overshoot and the dc current levels in order to comply with the widest span of manufacturers specifications on the write head and the magnetic medium. Also, the overshoot duration can be made adjustable by endowing the circuit with an appropriate delay generator.

Although this design was developed on the basis of the ST

Microelectronics 0.35-µm BiCMOS technology design kit, it is straightforwardly portable to full CMOS.

4.2 Circuit description

The proposed design is based upon a voltage-boosted architecture to the purpose of deriving the large overshoot current I_{OS} required for writing onto the medium (a little more than 100 mA through the head) from the low 3-V power supply. Power management considerations lead to discard the solution of definitely raising the supply voltage by means of an always-on converter, rather choosing to boost on the fly only when needed.

Figure 4.5 displays the blocks making up one quarter of the overshoot circuitry. As can be seen, the interconnect is tied to the inner nodes of the H-bridge MN_B, MP_B (the transistors on the right hand side not being shown): a reference bias V_{REF} is applied to the gates such that the switches stay turned off slightly under threshold, unless the voltage values on their sources fall out of the supply rails, that is, the related branches of the bridge are activated at pre-charge release. Figure 4.6 illustrates how the charge pump principle schematic works.

A programmable current-mirror reference (or DAC) formed by MN_{REF} and the logarithmic scale MN_{DAC0}, ..., $MN_{DAC(n-1)}$ is employed to set the overshoot current, followed by a separator (a low output impedance buffer) in order to properly drive the bridge without affecting the DAC's output voltage. An unbalanced logic inverter MN_{SW}, MP_{SW} connects the reference level to the gate of MP_{OS} acting as a multiplying current source. The latter is to be endowed with a very large aspect ratio W/L because of the considerable mirroring factor, even though this may be expensive in

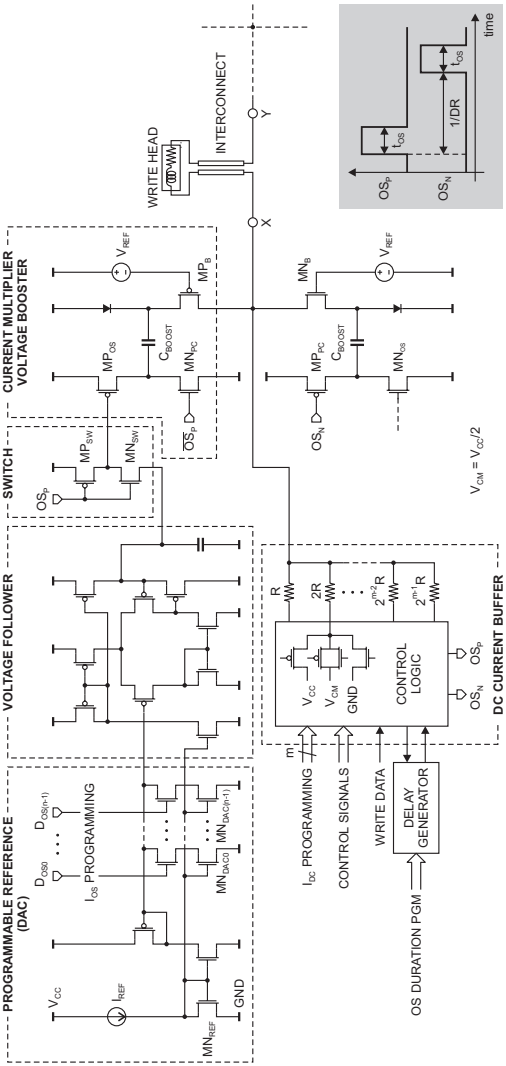


Figure 4.5 Circuit schematic of the write driver with the main blocks in evidence. Note the full-rate timing diagram on bottom right (*DR* = data rate).

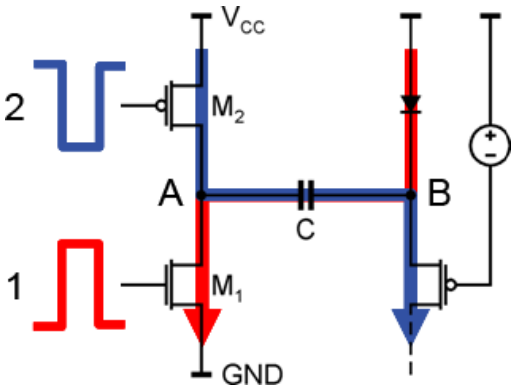


Figure 4.6 Principle diagram of the flying-capacitor circuit. 1. M_1 on, M_2 off: C is charged to $\sim V_{CC}$. 2. M_1 off, M_2 on: node A is raised to $\sim V_{CC}$ and node B goes to $\sim 2V_{CC}$, well beyond supply voltage.

terms of area.

Voltage boosting is implemented as follows. Via the diode and MN_{PC}, capacitor C_{BOOST} is pre-charged to V_{CC} (and similarly is its opponent on the other side) while not in use, that is, when current in the head is flowing the opposite way. At overshoot time both capacitors are switched so to swing the voltage across the bridge symmetrically out of the supply rails, theoretically tripling it (actually, peak voltage is only approximately doubled due to drops). Boost capacitors are chosen as result of a trade-off between power consumption, silicon usage, charging speed and pulse sustain capability: an acceptable compromise value sits around 50 pF.

The differential structure yields a common mode fixed at $V_{CC}/2$ at all times. It is worth noting that this layout also guarantees a prompt response when a write is initiated since all the capacitors are always kept charged, thus working out the issue of latencies.

As for the dc current, this is sourced by a second DAC made up of a logarithmic-scaled resistor ladder for I_{DC} programmability (see the left half of it in Figure 4.5): each resistance value is either inserted or detached by means of a three-way selector. Interconnect matching, i.e., holding a constant network impedance with varying bias conditions, is not pursued since several simulations proved it to be of no advantage to head current dynamics (because of the reasons discussed in the opening of this Section). The balanced design achieved by a switching scheme with two different voltage sources V_{CC} and V_{CM} again ensures the proper common mode level even for null I_{DC} without any drawback on consumption.

Eventually, some amount of support logic is added to handle the signals within the circuit itself. All the control signals and the programming codes, except write data, are to be exchanged with the host controller via a syncronous serial interface (neglected at this stage) and stored in a file of registers.

4.3 The low-power architecture

As apparent from Figure 4.5, the presented driver is made up of a sum of subcircuits, of which the bridge is but one part, although the most power-consuming. However, the bridge draws a variable current and only when a write cycle is in progress, whereas the other sections constantly dissipate, even when no write is being accomplished. This quantity can well reach a considerable share of the overall consumption: therefore, careful design is demanded in order to reduce the amount of power required to supply those parts.

In the present Section, the low-power enhancements adopted in the driver are described. These mark the actual improvement upon

the aforementioned references, which are either unconcerned with power optimization or do not account for it but within the bridge.

A first note is dealing with the currents drawn by each single branch along power rails. These quantities are optimally assigned the lowest values adequate for the task, that is, about a few hundred microamps, with the sole exception of the DAC's most significant bits. This is especially true of the reference value I_{REF}, being set at as low as 700 µA and subsequently elevated by a factor of one hundred through the bridge.

As previously evidenced, voltage boosting is not permanent; instead, it is performed on write request only, along with current multiplication. Morover, the arranged scheme allows for capacitors to be kept constantly on charge while not in use without causing any steady-state power consumption.

Noteworthy is also that the DAC circuit is not entirely reproduced four times alike: only one specimen is needed, together with just a bunch of current mirrors to drive the remaining branches of the bridge, which favors further reducing supply current.

The most important device introduced is probably the dc network being devised for a null overhead. The resistor ladder draws exactly as much as the provided dc current, which saves considerable power since I_{DC} is to be seamlessly sourced during a write.

4.4 Simulation results

The results of circuit simulation are shown in Figure 4.7: the boosted voltages and the write head current with varying codes are depicted at 250 Mbit/s (the rate of interest, also considering the interconnect features) for a given input string. It is apparent that the waveforms exhibit very neat shapes and peaks — only

the overshoot leading edge appears somewhat fuzzy and distorted in dynamics due to the presence of the interconnect, which is no issue since the peak current value is reached anyway. The graph also evidences the excellent linearity of both the overshoot and the dc currents versus the settings.

The used simulation engine is Eldo from Mentor Graphics, while the development was thoroughly performed under Cadence environment. A database model extracted from EM finite-element simulations of a reference commercial sample was adopted for the interconnect.

In Table 4.1, the mean dissipated power values are reported as a function of overshoot duration, while Figure 4.8 displays the waveform with both I_{OS} and I_{DC} set at their maximum, evidencing the effects of a variable overshoot duration on the write head current.

Table 4.1 Power dissipation with varying overshoot duration at I_{OS} = 100 mA, I_{DC} = 50 mA.

Overshoot duration *DUR* [ns]	Power dissipation P_D [mW]
1	303
2	444
3	554
4	605

4.5 Conclusions

In this Chapter, an enhanced low-voltage low-power inductive write head driver targeted to mobile hard disk drive applications

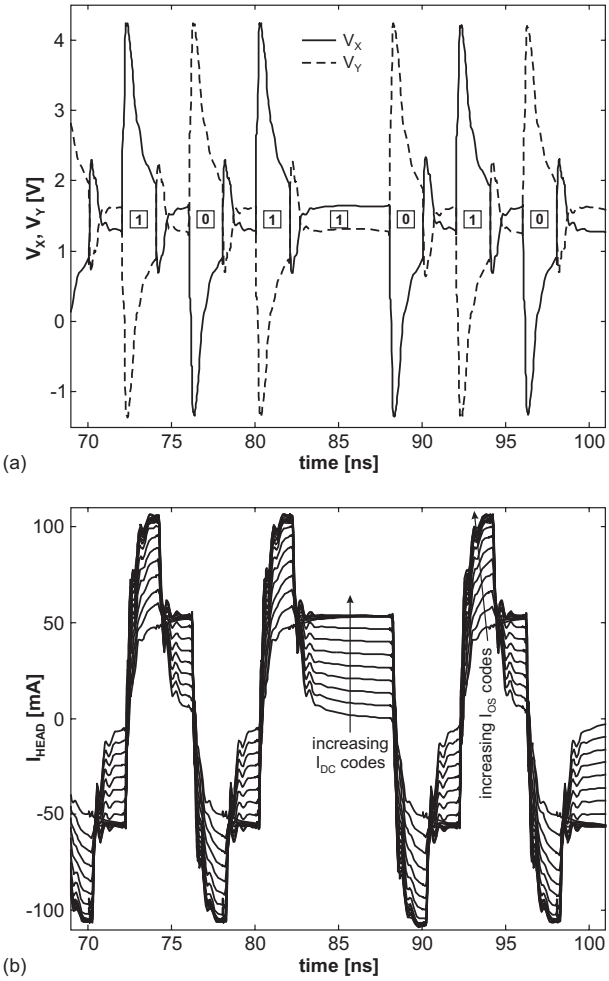


Figure 4.7 Overshoot voltages (a) and write head current with varying programming codes (b). The data being written appear boxed along the middle of (a).

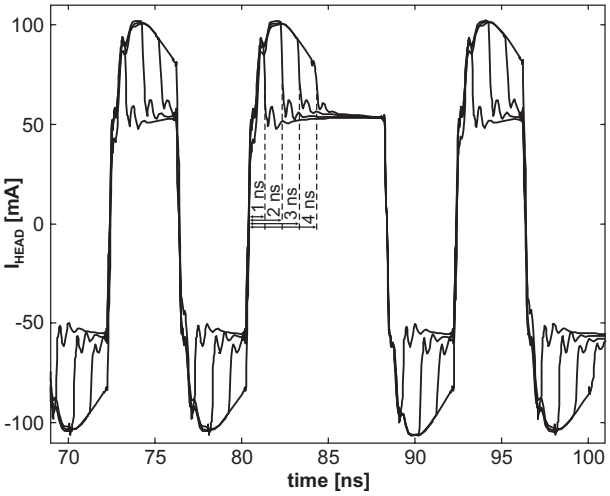


Figure 4.8 Current in write head with varying overshoot duration (maximum current levels; same write pattern as Figure 4.7).

has been demonstrated. A voltage-boosted architecture was proposed for operation from a 3-V single-ended supply, such as a battery, and accurate power optimization was performed, resulting in an average consumption around 440 mW at 250 Mbit/s data rate. Moreover, the circuit was designed to be thoroughly programmable as to the overshoot and the dc currents (up to 100 and 50 mA respectively) as well as the overshoot duration (in the span $1 \div 4$ ns) for commercial compliance purposes. The write driver was developed using 0.35-μm BiCMOS technology; however, effortless portability to full CMOS065 was pursued at design stage.

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